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A Burst Compression and Expansion Technique for Variable-Rate Users in Satellite-Switched TDMA Networks

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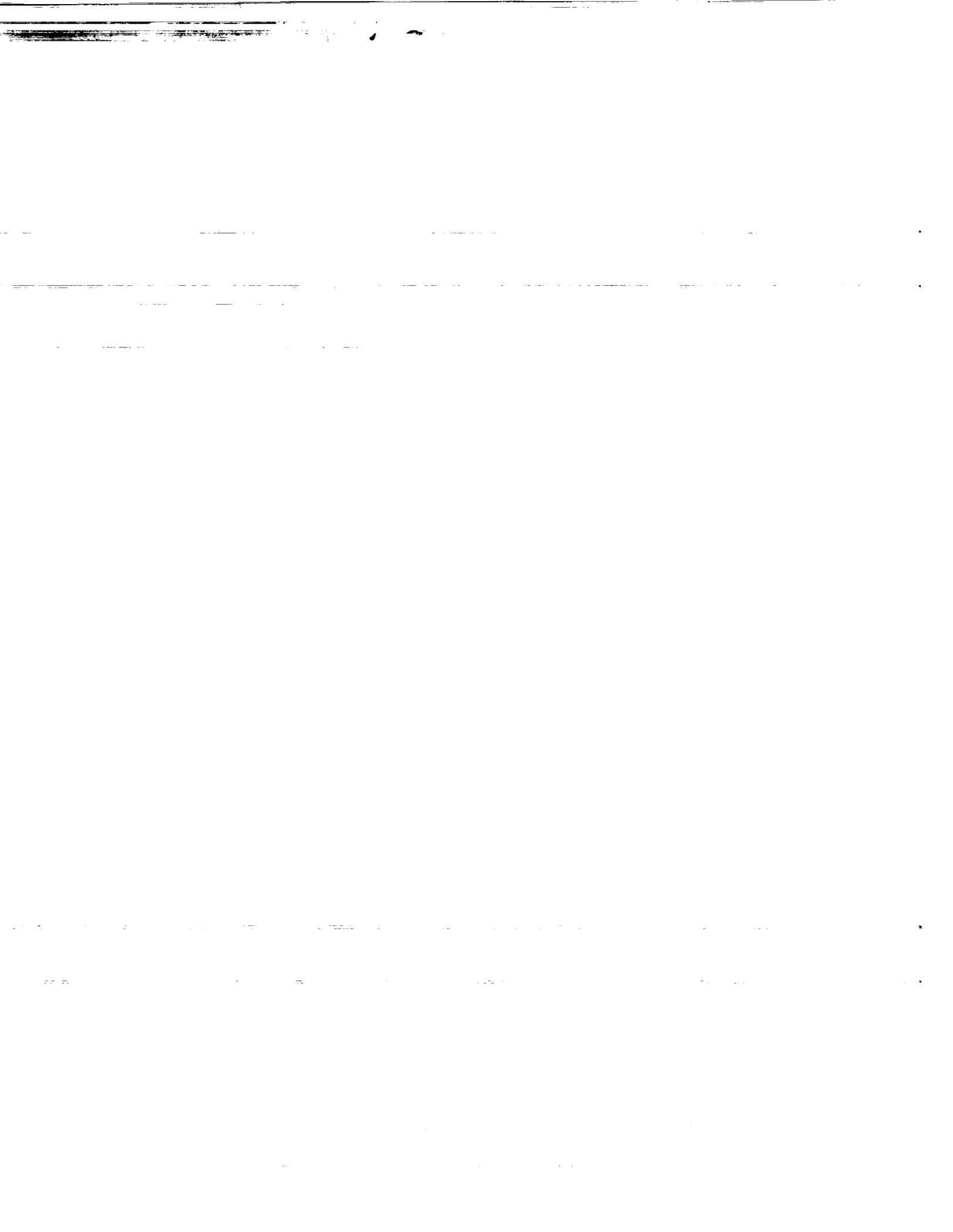
(NASA-TM-102414) A BURST COMPRESSION AND
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A BURST COMPRESSION AND EXPANSION TECHNIQUE FOR VARIABLE-RATE USERS IN SATELLITE-SWITCHED TDMA NETWORKS

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Abstract

A burst compression and expansion technique is described for asynchronously interconnecting variable-data-rate users with cost-efficient ground terminals in a satellite-switched, time-division-multiple-access (SS/TDMA) network. Compression and expansion buffers in each ground terminal convert between lower rate, asynchronous, continuous-user data streams and higher-rate TDMA bursts synchronized with the satellite-switched timing. The technique described uses a first-in, first-out (FIFO) memory approach which enables the use of inexpensive clock sources by both the users and the ground terminals and obviates the need for elaborate user clock synchronization processes. A continuous range of data rates from kilobits per second to that approaching the modulator burst rate (hundreds of megabits per second) can be accommodated. The technique was developed for use in the NASA Lewis Research Center System Integration, Test, and Evaluation (SITE) facility. Some key features of the technique have also been implemented in the ground terminals developed at NASA Lewis for use in on-orbit evaluation of the Advanced Communications Technology Satellite (ACTS) high burst rate (HBR) system.

Introduction

Satellite-Switched TDMA

Time-division-multiple-access (TDMA) is a technique whereby network users with different data throughput requirements can equitably and efficiently timeshare the network resources. In a satellite-switched TDMA (SS/TDMA) network, communication among geographically dispersed users is enabled through an onboard crosspoint, or matrix switch. The matrix switch routes the bursts of source user data that are received via uplink antenna beams to downlink beams that illuminate the areas where destination users are located. The bursts are timed so that only one pair of source and destination users are communicating at any instant in time. For the duration of their burst, the full receiving, switching, and transmitting resources of the satellite are allocated to them. These resources are divided or time-division-multiplexed among all active users in the network.

Greater flexibility in interconnecting widely dispersed users is enabled through the use of hopping beams. Here, multiple uplink and downlink antenna beams are electron-

ically switched to cover specific source and destination locations simultaneously in a periodic sequence. Source and destination users in covered locations communicate with each other through TDMA ground terminals (see Fig. 1). The Advanced Communications Technology Satellite (ACTS) under development by the NASA Lewis Research Center will demonstrate the flexibility of SS/TDMA using multiple hopping beam antennas.¹ For more information on TDMA systems architecture and terminal implementation see Ref. 2.

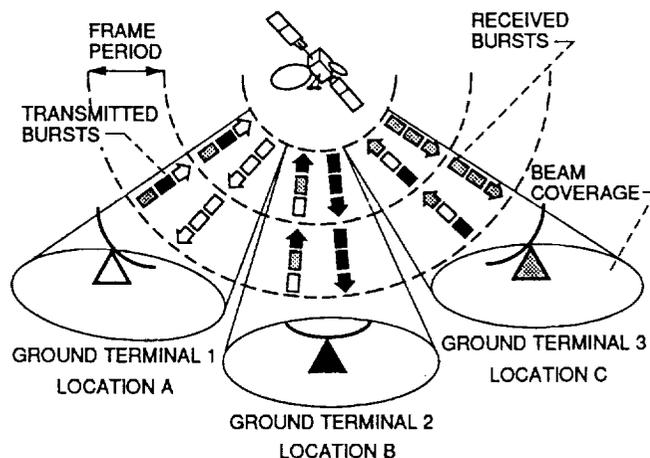


Fig. 1 Multiple-beam, satellite-switched, time-division-multiple-access (SS/TDMA) network.

A precise method for maintaining timing and synchronization among users, their TDMA terminals, the hopping satellite antennas, and the onboard matrix switch is required in order to enable the sequential communication among multiple users across the network. This paper addresses a technique for maintaining timing and synchronization among users who have variable-data-rate requirements and the TDMA network ground terminals. In this introductory section, the concept of burst-time plans and TDMA frames is briefly explained, followed by a description of the role of compression and expansion buffers in a TDMA terminal. The rationale for supporting variable-data-rate users is provided next, and the section concludes by noting current and potential applications. In subsequent sections of the paper, an overview of the technical approach and its advantages are presented, followed by a discussion of the sources of clock variation in an SS/TDMA system and methods used to accommodate them.

Specific objectives and details of how the variable-rate burst synchronization technique meets those objectives are presented in the final section.

Burst-Time Plans

Burst transmissions from all source terminals are time-multiplexed over the course of a TDMA frame (typically 1 to 30 ms in duration) to arrive at the satellite in synchronism with the matrix switch timing. To ensure that only one burst arrives at the satellite in each time slot, the timing of burst transmissions is coordinated through a predetermined burst-time plan (BTP) established by a network control computer attached to a master control terminal. The BTP consists of transmit and receive time slot assignments for each terminal in the network. The BTP repeats every TDMA frame and is updated when users place new connection and disconnection requests. For further information regarding the generation of BTP's for a TDMA system see Ref. 3.

Compression and Expansion Buffers

At each source terminal, continuous digital data streams from multiple users are compressed into high-rate bursts for modulation and transmission at the assigned time slots within the TDMA frame (see Fig. 2). Serial data from each source user are temporarily converted to a parallel format and stored in one of several compression buffers. At the assigned time, parallel data are read out of the compression buffer onto the transmit multiplexed data bus, scrambled, converted to a high-rate, serial data format, and modulated as a burst. Scrambling (for the purpose of energy dispersal within the modulated spectrum) is accomplished by "exclusive ORing" the user data with a known pseudorandom sequence on a bit-by-bit basis. Bursts received by the destination terminal are converted back to a parallel format, descrambled (to restore the original data sequence), and expanded back into continuous data streams at the original lower data rates and delivered to the destination users.

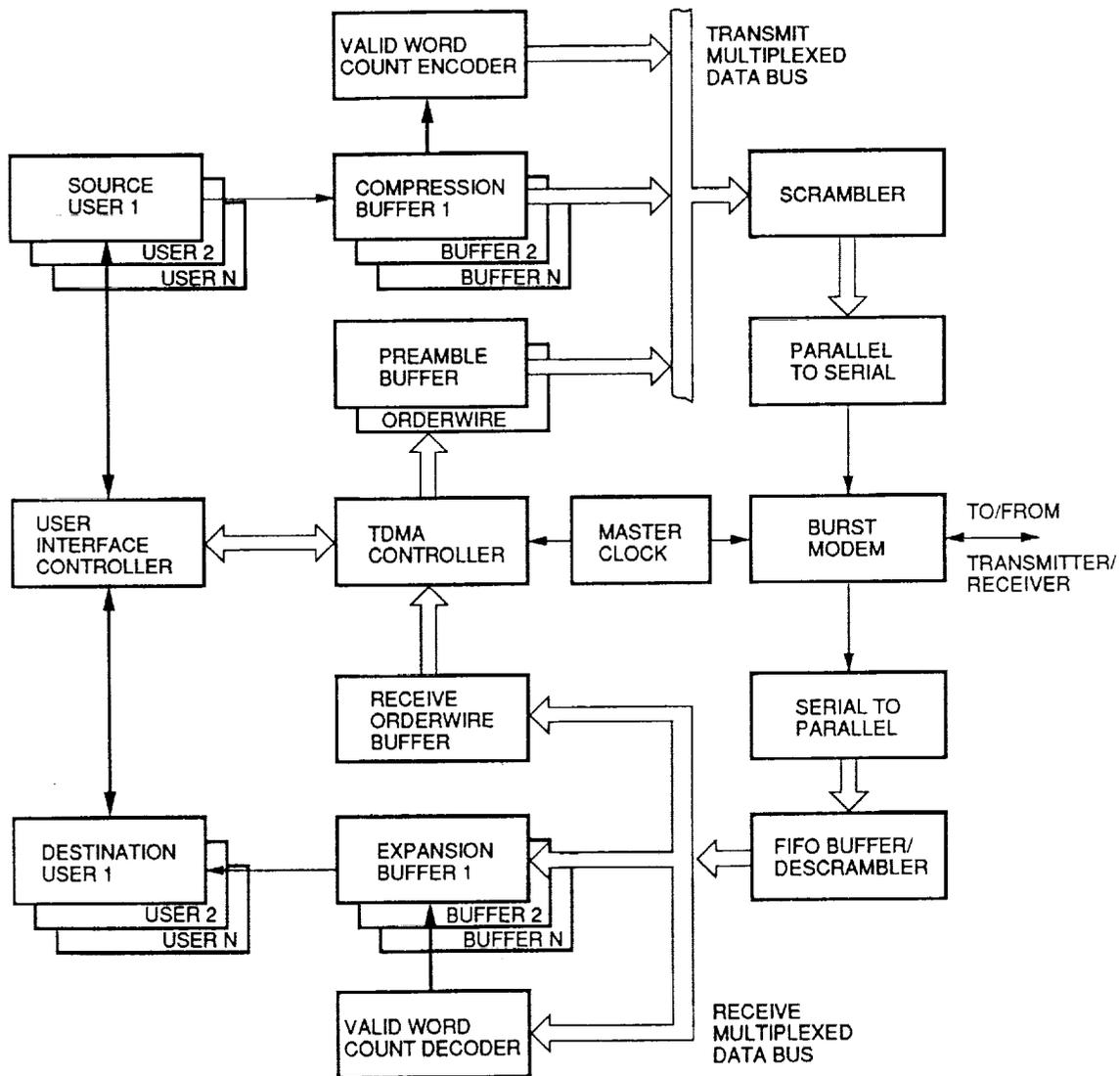


Fig. 2 TDMA ground terminal block diagram.

Compression buffers on the transmit side of the TDMA terminal and expansion buffers on the receive side are used (1) as an interface between the continuous, low-rate data streams of each user and the high-rate burst modem, (2) to enable corrections in transmit burst timing and absorb variations in receive burst timing to compensate for satellite motion, and (3) to absorb variations in instantaneous data rates caused by asynchronous clocks, oscillator instability, and satellite-motion-induced Doppler frequency shifting.

In the terrestrial interface equipment of a TDMA terminal, compression and expansion buffers can be implemented with either "ping-pong" (on-line, off-line) memories or "first-in, first-out" (FIFO) memories. Ping-pong memories are two banks of memory operating in parallel (see Fig. 3(a)). When one bank is being written into at one data rate, the other can be read from at another data rate. The figure depicts the condition when input data are written into "ping" while output data are read from "pong." At the end of each TDMA frame, the state of the control lines is switched and the two banks of memories are ping-ponged. The data written into one bank during the previous frame can then be read out during the current frame.

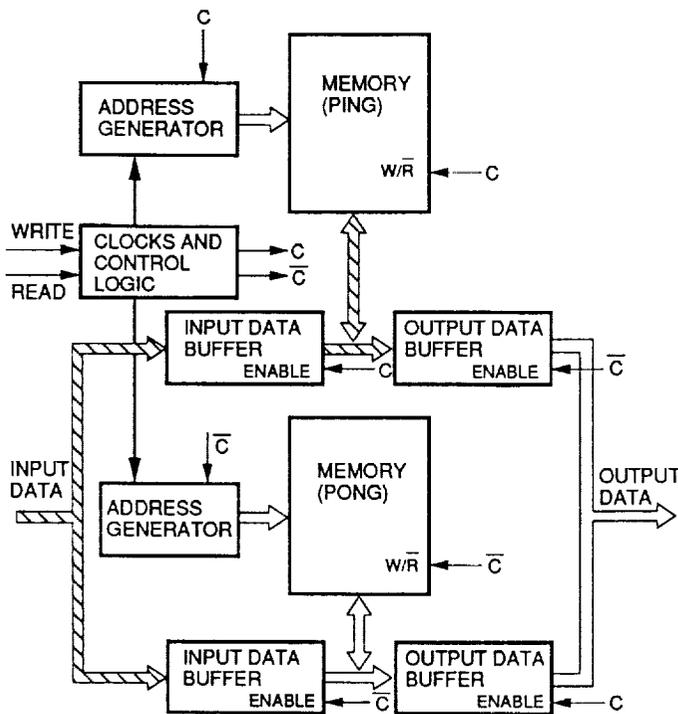


Fig. 3(a) Simplified block diagram of "ping-pong" buffer memory.

In contrast, FIFO memories appear externally to be dual-ported, elastic storage devices (see Fig. 3(b)). Data written into a FIFO memory sequentially at one rate can be read out in the same sequence at a different rate without external generation of write and read addresses.

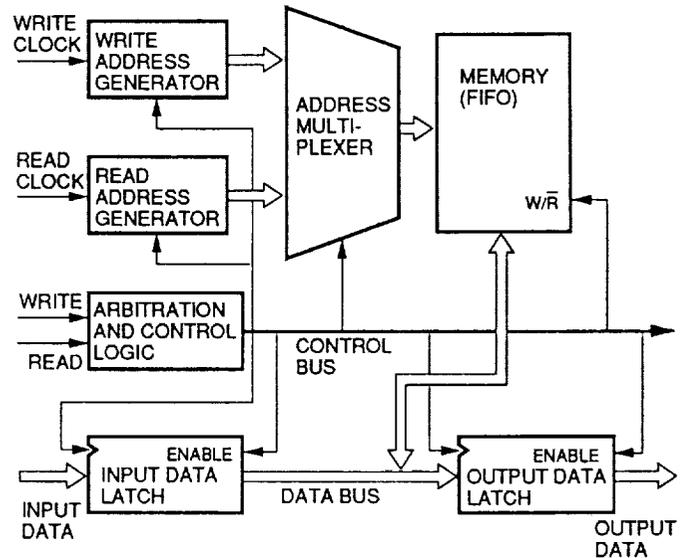


Fig. 3(b) Simplified block diagram of FIFO buffer memory.

Only half of the memory locations and data buffers required for a ping-pong implementation are needed for the same data throughput capability in a FIFO memory implementation. Even though the amount of integrated circuit memory is no longer considered to be a cost driver in digital systems, the FIFO memory approach to compression and expansion buffer implementation offers several advantages over the ping-pong memory approach. The most significant of these is its ability to support asynchronous, variable-rate users with minimal data latency (delay within the buffer memory itself). Internal arbitration between the FIFO memory's write and read cycles, and the sequential flow of data through a shallow FIFO memory, are the two key features exploited by the variable-data-rate compression and expansion buffer technique described in this paper.

Variable-Rate Users

In many TDMA satellite networks, only user data rates that are nearly synchronous submultiples of the network master clock can be accommodated. In addition, the frequency of both the user and terminal clocks must be controlled to an accuracy and stability of typically $\pm 10^{-6}/s$.⁴ To ensure proper burst arrival time at the satellite, the ground terminal may be required to synchronize its modulator burst clock to a network master clock having a stability of $\pm 10^{-8}/s$ or higher. For a high-efficiency TDMA system with burst rates of several hundred megabits per second, synchronization to a master clock to within $\pm 10^{-10}/s$ may be required. In general, for a given stability, the cost of an oscillator increases with its output frequency. An SS/TDMA network that supports a continuum of user data rates (from tens or hundreds of kilobits per second to nearly the modulator burst rate), all of which are asynchronous with the network master clock, and places minimal requirements on short- and long-term clock accuracy and stability (typically $\pm 10^{-4}/s$), can provide a

variety of new communications services and reduce traffic terminal production and maintenance costs. At the same time, all other terminal subsystems can operate in synchronism with a single master clock, free-running at the modulator burst rate. A variable rate, burst compression and expansion technique is required to realize this potential.

In the technique described in this paper, all user data are transferred to and from the ground terminal as continuous, serial data streams regardless of the information rate, content, format, or framing. The source users' bit clocks are asynchronous with respect to the terminal's single master clock. TDMA networks are well suited to communications with high data throughput (hundreds of megabits per second). TDMA frame formats and terminals designed to exploit the flexibility of this technique will extend many of the advantages of TDMA communications to a wide range of low-to-medium data rate users (hundreds of

kilobits to a few megabits per second) with low-cost digital terminals.

Applications

The variable-rate burst compression and expansion buffer technique was developed to enable a variety of communications experiments via NASA Lewis' in-house Systems Integration, Test, and Evaluation (SITE) facility, an SS/TDMA network hardware simulator/demonstrator.⁵ The technique was implemented for three source and destination users in each of the SITE TDMA ground terminals (see Fig. 4(a)). The salient features of the technique have also been applied in the Link Evaluation Terminal (LET) under development at NASA Lewis (see Fig. 4(b)) to characterize the on-orbit bit-error-rate performance of the matrix-switched, high burst rate (HBR) segment onboard the ACTS.

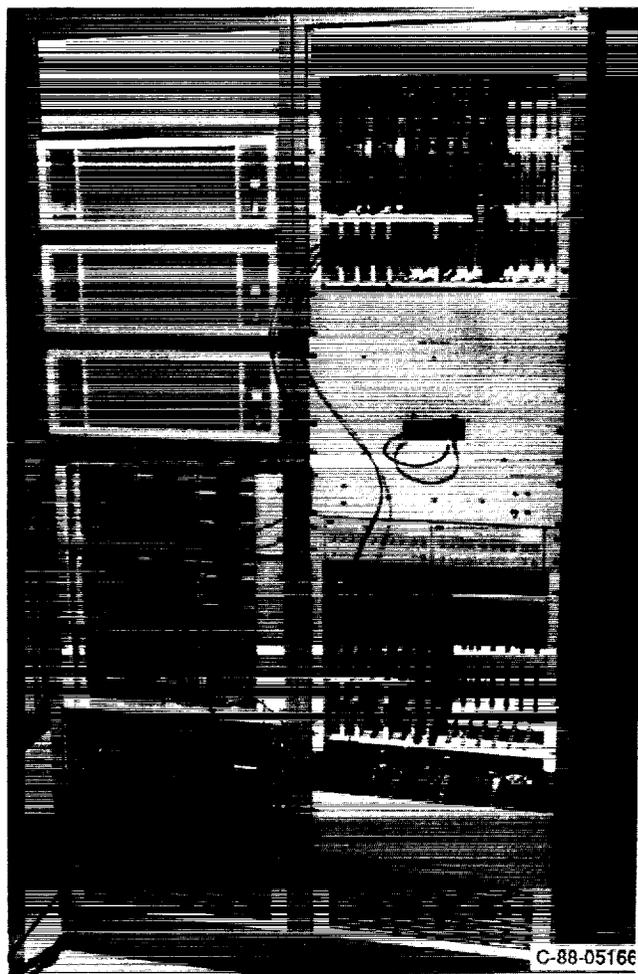


Fig. 4(a) Lewis' site project TDMA ground terminal.

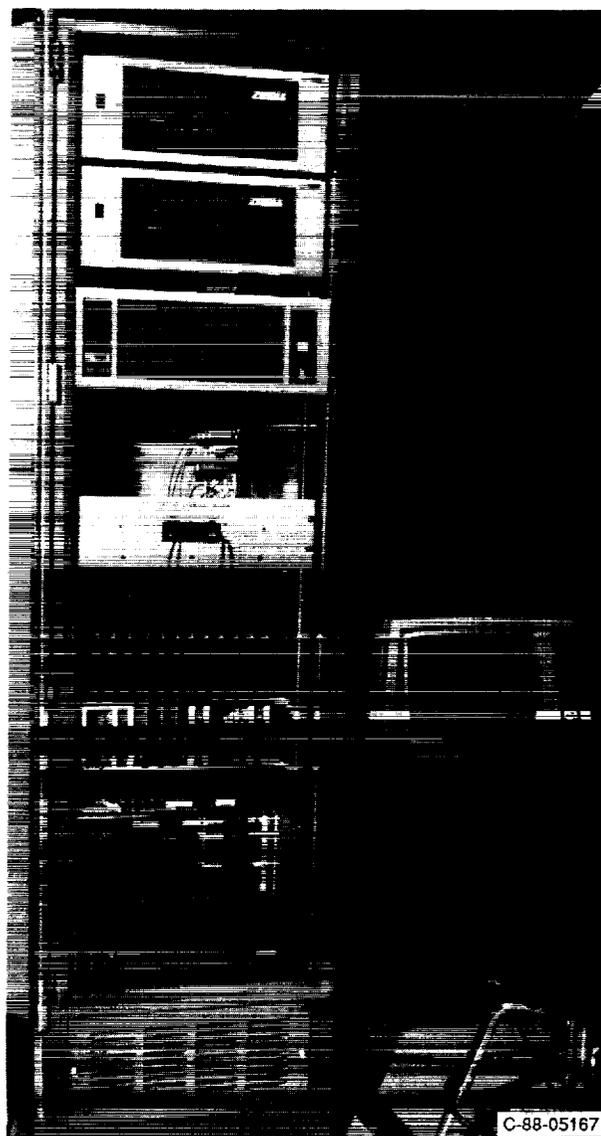


Fig. 4(b) Lewis' link evaluation terminal (LET) for on-orbit characterization of the ACTS.

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The technique is also suitable for use in packet-switched networks with variable-length data packets where the slight additional overhead required for its implementation could be included in the packet headers. Hardware demonstration models for a processing satellite network with onboard packet-switching capability will be developed in future phases of the SITE project. Implementation ease and cost efficiency of digital ground terminals and experiment flexibility were the major development goals. Expanded user support capabilities and reduced requirements on user and terminal clock accuracy, stability, and synchronization processes are the byproducts of the development.

Technical Approach

An intrinsic requirement of SS/TDMA networks is to maintain precise control of timing and synchronization across the network in order to effectively and efficiently utilize the ground and space resources. Network users with the need for communications services at a variety of asynchronous data rates present a challenge to the designers of TDMA terminals -- how can an inherently synchronous space communications system appear to be nearly transparent to the asynchronous user? In this section, the salient features of the variable-rate compression and expansion buffer technique are presented along with some advantages the technique offers to existing and potential service users.

Variable-Rate Technique Overview

To support multiple users with a wide range of asynchronous data rates, the number of bits of user data transmitted by the source terminal from frame to frame must vary. At the destination terminal, the regenerated bit clock delivered to the user must replicate the frequency and stability of the source user. The key feature of the technique is to group the number of lower rate user data bits received by the source terminal over roughly one frame period into an equivalent number of higher bit rate valid data words per frame and thereby "quantize" the frame-to-frame variation in the number of valid data bits per frame into one-word increments. This grouping of user data into words is performed by the compression buffer; continuous user data are written into the FIFO memory at the user's clock rate and are read out at the burst modulator clock rate. Each transmitted burst is an integer number of words in duration. On a frame-to-frame basis, the number of valid words in the burst may increase or decrease by one from some nominal number that represents the approximate data throughput.

Every continuous data rate (in bits per second) within the supported range of rates is converted into an equivalent number of valid data words per frame. The word width internal to the ground terminal is a function of the data rates to be processed and the speed of available memory. The integer portion of the number of valid data words per frame is referred to as the nominal word count (NWC) (see Fig. 5). The source terminal inserts a short codeword,

called a valid word count (VWC), in front of each data burst to inform the destination terminal if the number of valid words in the burst is different from the NWC value it is expecting. For example, before the source user begins sending data, none of the words in the burst are valid and the VWC indicates this condition. Transmission of valid bursts (NWC in duration) will not begin until a number of words at least equal to the NWC is available in the compression buffer. During each transmit frame, additional bits beyond the integer number of valid words (the NWC) accumulate in the compression FIFO buffer of the source terminal, thus increasing the relative "fill level." This continues until enough bits have accumulated during some later frame to form an additional word, which can be transmitted along with NWC valid words during the next frame. The VWC preceding that burst will then indicate that one word more than the NWC has been transmitted.

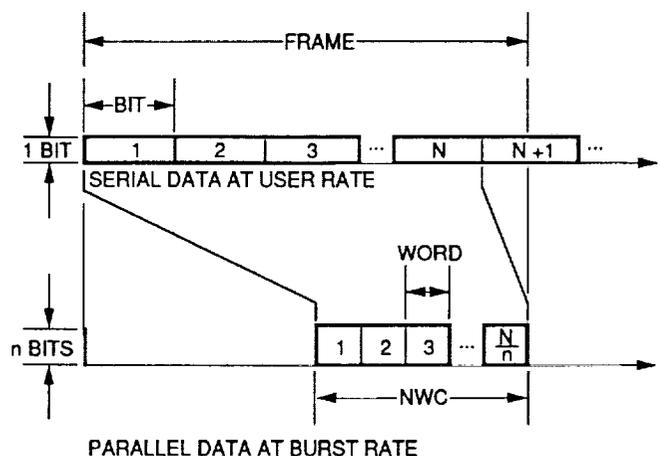


Fig. 5 Conversion of continuous valid data bits to an equivalent number of valid data words per frame.

The BTP for the source and destination terminals, as well as the onboard matrix switch state tables, must reflect an assignment of a time slot several words longer in duration than that required to transmit the NWC alone. The assigned time slot must be long enough to contain the burst overhead bits (the demodulator preamble and a guard time between bursts), and one additional word to accommodate periodically both the decimal fraction of valid words per frame and any user clock frequency variations. In practice, the TDMA frame may be partitioned into smaller subframes of a convenient number of words in duration to ease BTP assignments. In such a case, the smallest number of subframes that contain the longest possible burst for that data rate (including TDMA overhead) are assigned (see Fig. 6).

The accumulation of continuous user data in the compression buffer over one frame (before, during, and after burst transmission) is depicted in the graph shown in Fig. 7. The effect of bit and word quantization on fill level is removed for clarity.

In the destination terminal, a control loop subroutine executing in the user interface controller varies the frequency of a voltage-controlled oscillator (VCO). The VCO

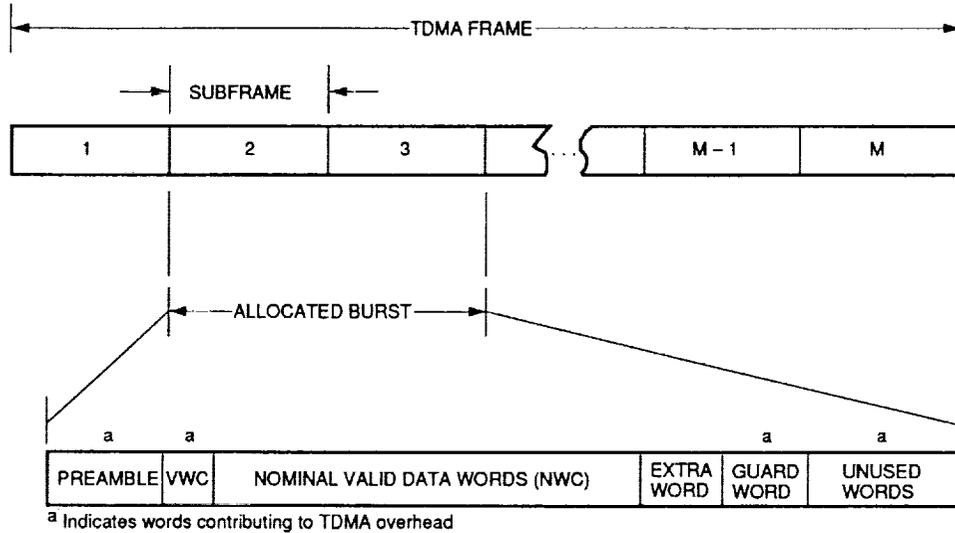


Fig. 6 Burst allocation in a TDMA frame partitioned into M subframes.

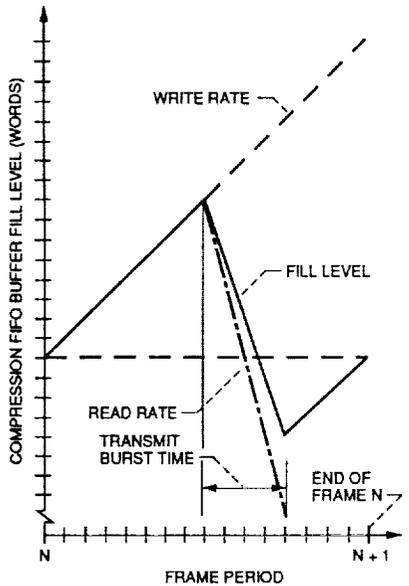


Fig. 7 Compression buffer fill level over one frame.

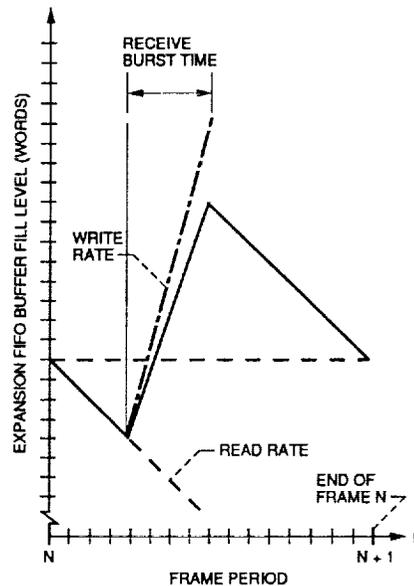


Fig. 8 Expansion buffer fill level over one frame.

is used to generate the read clock for the expansion FIFO buffer and the data synchronized bit clock delivered to the destination user. The control loop adjusts the regenerated clock frequency based on the fill level of the expansion FIFO buffer observed at the end of each frame. The level of valid data in the expansion buffer is depicted in Fig. 8.

The microprocessor-controlled clock regeneration loop creates a smoothed bit clock for the destination user with equal or better stability than that of the source user bit clock. At the same time, the finer satellite-motion-induced frequency variations are absorbed with compres-

sion and expansion buffer memories significantly smaller than those necessary for techniques that require nearly synchronous user and terminal clocks.

Advantages

In contrast to conventional pulse-stuffing techniques used to convey information about valid data content from source to destination, this technique does not require serial data processing at the full user data rate (as is required in stuff and destuff controllers). Because the NWC is known at the destination terminal (from the BTP) and because the

VWC codeword can be error encoded, the technique significantly reduces the decoding errors introduced during pulse destuffing techniques. This technique also avoids the abrupt, short-term timing jitter introduced by conventional pulse stuffing at prescribed time locations.

The variable data rate, compression and expansion buffer technique, as designed for TDMA terminals of the SITE facility, accommodates any user data rate from 256 kb/s to nearly the 221 Mb/s modulator burst rate. User data are delayed by no more than two frame periods in each buffer regardless of the information bit rate. Minimal additional bits are added to the TDMA overhead. The variable-rate buffer technique readily absorbs user bit clock instability (as poor as $\pm 10^{-4}$ /s) and the fine satellite-motion-induced Doppler shift (on the order of $\pm 10^{-9}$ /s) without generating slips in frame timing. The relaxed clock stability requirement and asynchronous operation offer ground segment cost savings and data rate flexibility unavailable to SS/TDMA networks that require synchronous or nearly synchronous operation.

Sources of Clock Variation

The TDMA terminal's compression buffers must absorb or otherwise accommodate apparent timing and frequency variations in the serial data rate received from the source users. Likewise, the expansion buffers must accept similar variations in the arrival time and frequency of the high-bit-rate bursts received via the satellite. The variation in range between the on-orbit satellite and the ground terminals is the primary source of clock or timing variation. The two primary sources of frequency variation in a SS/TDMA system are the rate at which the range delay varies and the oscillator imperfections. Frequency variation from any source can also lead to bit and frame timing variation with respect to a clock at the destination. The consequences of each of these sources of variation and their effect on the design and implementation of compression and expansion buffers will be discussed in the sections that follow.

Range Delay Variation

Compression and expansion buffers can be used to absorb the bit timing fluctuations caused by variation in the distance between the terminal and the satellite. The nominal distance or "range" between a ground terminal and a satellite in a geostationary orbit (a circular orbit of radius 42 242 km that is lying in the Earth's equatorial plane) can be computed from a set of orbital mechanics equations for a specific location on the surface of the Earth.⁶ The average range between NASA Lewis' geostationary satellite ACTS (to be located at 100° west longitude), and the closest and farthest major cities in the contiguous 48 states is expected to be about 37 660 km.⁷ A signal traversing this distance at the speed of light would experience a nominal range delay of about 125 ms. For a typical satellite link, variations in the range delay over a 24-hr period (primarily due to orbit inclination, eccentricity, and atmospheric and ionospheric variations) can

reach a maximum value on the order of a few milliseconds.⁸

More tightly station-kept processing satellites with multiple-beam antennas like the ACTS will yield significantly lower maximum range delay variation. For example, the maximum range delay variation (in seconds) is equal to the nominal maximum range variation over one day, d_{\max} (in meters), divided by the velocity of propagation, c (in meters per second):

$$T_d = d_{\max}/c$$

For the ACTS, a nominal maximum range variation of ± 20 km has been specified. Therefore, the maximum range delay variation is:

$$T_d = 40 \times 10^3 \text{ (m)} / 3 \times 10^8 \text{ (m/s)} = 133 \times 10^{-6} \text{ s}$$

The number of bits of compression and expansion buffer memory, N_v , necessary to accommodate the range delay variation at a data throughput equal to the modulator burst rate is the maximum range delay variation, T_d (in seconds) divided by the modulator bit period, T_b (in seconds per bit):

$$N_v = T_d/T_b$$

The modulator burst rate used in both the ACTS link evaluation terminal (LET) and the SITE facility is 221.184 Mb/s. T_b is the inverse of this rate, or 4.52 ns/b. So for this burst rate:

$$N_v = 133 \times 10^{-6} \text{ (s)} / 4.52 \times 10^{-9} \text{ (s/b)} = 29.4 \times 10^3 \text{ b}$$

Hence, it would appear that modest 32 kb memories would be sufficient for the compression and expansion buffers in any TDMA terminals to communicate via the ACTS using a burst rate of 221.184 Mb/s. If the range delay variation had been closer to that of the typical satellite, say 10 ms for example, the same burst rate would have required buffers with over 2 Mb of storage each. While neither of these examples presents a difficult or costly memory requirement, the problem with this approach to buffer design is that burst transmission cannot begin until the compression buffer reaches the half-full level at the midpoint of the range delay variation. If the compression buffer is not filled to this point, then, as the satellite moves away from the source terminal and burst transmission occurs earlier (to insure correct arrival time at the satellite), the compression buffer will be gradually depleted until it is empty. This will result in a burst containing invalid data. Conversely, if the half-full condition is not established at the correct time, the buffer can just as easily overflow as the satellite continues to move toward the source terminal. A similar condition must be established in the expansion buffers at the destination terminal.

The impact of delaying user data in conventional compression and expansion buffers until the half-full condition is reached becomes severe for low-data-rate users because

the buffers must be designed to accommodate the maximum data throughput (nearly the modulator burst rate) and it may take hundreds of TDMA frames before transmission can begin. However, by using the variable-rate burst compression and expansion technique, the fill level is set according to the user's data rate to minimize data delay within the ground terminal. The fill level is roughly proportional to the ratio of the user's data rate to the modulator burst rate. Each data rate experiences the same throughput delay as all others.

Variable Frame Duration Technique

To accommodate the effect of range delay variation on TDMA frame timing a second technique is used. Each terminal autonomously adjusts its transmit and receive frame duration to ensure proper burst timing at the satellite (see Fig. 9). As the range for a specific terminal decreases, it will simultaneously increase its transmit frame counters 1-bit period at a time (thereby delaying its burst transmission), and decrease its receive frame counters by 1-bit period as well (thereby anticipating the early arrival of the burst). The opposite adjustment takes place for an increase in range delay. This technique requires that a portion of each source terminal's burst transmission be looped back to that terminal for closed-loop timing adjustment.

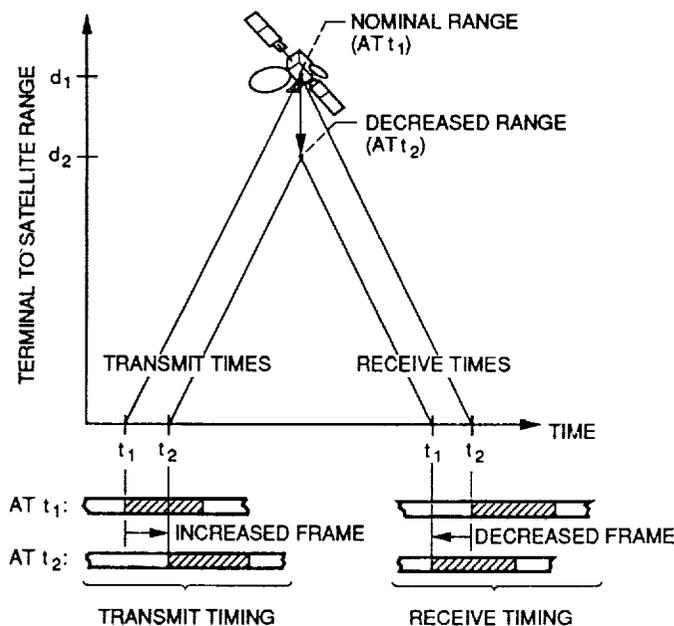


Fig. 9 Ground terminal transmit and receive frame duration adjustment to maintain burst timing during range variation.

Occasionally increasing or decreasing the frame counters by 1-bit count is accomplished through a variable count word generator (VCWG). By using the ground terminal's single high-speed clock (the modulator input bit clock), the VCWG can create word edges with 63-, 64-, 65-, or 56-bit periods per word. The transmit and receive frame counters can insert a 1-bit shortened (63-bit), normal (64-bit), or 1-bit extended (65-bit) word as the unused "guard word" at

the end of the frame. During initial TDMA terminal acquisition, this variable frame duration technique is also employed to reduce the complexity of ground terminal and onboard matrix switch timing synchronization. There, the VCWG is set to provide an 8-bit shortened (56-bit) word at the end of each frame. This coarse timing adjustment is used to search for correct timing with respect to reference bursts transmitted by a master control terminal.

The burst demodulator has the ability to produce correct data as long as the burst arrives within some timing window, typically on the order of tens of bits in duration. Any burst arrival time variance acceptable to the demodulator but not compensated for by the variable frame duration technique is absorbed in a shallow FIFO buffer that precedes the descrambler. Only a few words deep on average, a single FIFO buffer at this location enables all expansion buffers attached to the received data multiplexed bus to operate in synchronism with the terminal's master clock (see Fig. 2).

If this technique is used, only one master clock is required for each terminal, and with self-adjustment of burst timing, the ground terminal's single oscillator can operate with minimal frequency adjustment (to correct only long-term aging effects). This technique is used in both the SITE ground terminals and the LET. Under the SITE project, a range delay simulator capable of fixed and variable delay of data at the modulator burst rate was developed.⁹ The range delay simulator is used to evaluate the performance of this technique. Further details of the variable frame duration technique are beyond the scope of this paper. Nevertheless, by using this technique, range delay variation is handled effectively with minimal depth buffer memories and uniform data transport delay through the ground terminal.

Rate of Range Delay Variation

The destination terminal must absorb the apparent frequency variations caused by Doppler shifting of the signal through the moving satellite. The rate of range delay variation determines the apparent shift in received frequency at the destination terminal. The received frequency shift will be different for bursts received from different users since each source terminal will experience a unique uplink range variation. The satellite may be moving toward one source terminal at the same instant it is moving away from another. An additional Doppler shift (likely to be different in magnitude and/or direction from the uplink Doppler shift) will be imposed on all downlink bursts received at each destination terminal based on specific range delay variation experienced by that terminal. Doppler shift in frequency of the received bursts is indistinguishable from the inaccuracy and instability of each source terminal's modulator burst oscillator (an oven-stabilized, voltage-controlled crystal oscillator (VCXO) operating at 221.184 MHz). The magnitude of the Doppler shift, like the oscillator instability at that high a frequency, is quite small (on the order of a few nanoseconds per second).

The frequency shift of bursts received by the destination terminal is minimal if the satellite is moving at the same rate in opposite directions from the source and destination terminals. It is maximal for the opposite condition. The maximum clock frequency variation due to Doppler shift, F_D (expressed in bits per second), is equal to twice the maximum satellite range rate, R_r (in meters per second), times the modulator burst rate, R_m (in bits per second), divided by the velocity of propagation, c (in meters per second):

$$F_D = 2R_r R_m / c$$

The maximum range rate specified for the ACTS is ± 1.2 m/s and the modulator burst rate is once again 221.184 Mb/s. Therefore:

$$F_D = 2(1.2)(221.184 \times 10^6) / (3 \times 10^8) = 1.77 \text{ b/s}$$

At the maximum rate of range variation, a 1-bit period appears to accumulate or to be depleted every $1/F_D = 0.56$ s. With a frame duration of 1 ms, it takes at least 1770 frames for the variation to be observed. Over a 12-hr period, however, a ground terminal in the ACTS network may observe as much as 30 km of variation in range. At a burst rate of nominally 220 Mb/s, about 22 kb appear to accumulate or be depleted over that time. An important feature of the variable-rate compression and expansion buffer technique used in conjunction with the variable frame duration technique is that the subtle yet cumulative effects of Doppler shift and modulator clock inaccuracy and instability are readily absorbed without modification to the design.

User Clock Imperfections

One of the primary reasons for the development of the variable-rate compression and expansion buffer technique was to enable the use of inexpensive user bit clock sources with no frequency control loop across the user/ground terminal interface. The ground terminal will accept the source user's digital data stream and synchronized bit clock, and deliver the same digital data stream and a regenerated, synchronized bit clock to the destination user. To process the serial data streams in this fashion, the compression buffer must absorb the frequency inaccuracies and instabilities of the users' bit clocks within some minimal specification limits.

Any oscillators used to generate bit clocks will exhibit some level of degradation from ideal oscillators in three significant parameters:

- (1) Accuracy - how close the oscillator output frequency is to a desired frequency;
- (2) Reproducibility - how well two sources can be adjusted to generate the same frequency, or one source can repeatedly generate the same frequency; and
- (3) Short- and long-term stability - frequency variation over time due to random internally generated noise

and drift created by component aging and temperature effects.

The cost of a clock-generation subsystem increases with increasingly stringent specifications on each of these three parameters. The least expensive approach allows for free-running oscillators in the source user's equipment, moderately accurate and stable modem oscillators, and simple control loops in the clock regeneration subsystem of the destination terminal.

When applied to the design and development of the TDMA ground terminal's terrestrial (user) interface equipment, the measure of these performance parameters is somewhat different than those specified by commercial oscillator manufacturers. Stability is typically measured over 1 s for the short-term parameter and over 1 day for the long term. In the TDMA user interface, short-term stability is relative to the TDMA frame duration. The ground terminal has the opportunity to "resynchronize" its counters at TDMA frame boundaries. In the short term, an oscillator need only meet a specified stability over one-frame period, typically tens of milliseconds. Over such a short period, temperature stability is of no consequence. Typical frequency stability over a temperature range of 0 to 50 °C for crystal oscillators varies from $\pm 10^{-6}$ in uncompensated products to $\pm 10^{-9}$ for oven-controlled packages.^{10,11} Over a short term on the order of hundreds of milliseconds, $\pm 5 \times 10^{-11}$ stability is achievable. The effects of long-term stability, accuracy, and reproducibility are indistinguishable from each other in the proposed variable-rate technique. Adjustments in the amount of valid data contained in a burst from the source terminal, along with the control loop used to regenerate the user clock in the destination terminal, treat the observable effect of these degradations identically.

Timing Slips

The TDMA terminal is required to absorb or otherwise control the significant effects of bit and frame timing slips on the digital data stream. These slips occur when phase alignment cannot be maintained between two clocks across an interface - in this case, between the terrestrial user and the TDMA terminal. The result of a timing slip is either a bit insertion or deletion into or out of the digital data stream. Neither condition is desirable from a user's standpoint, but if well-controlled and documented, either may be acceptable. The variable-rate compression and expansion technique circumvents the timing slip condition completely.

One common but expensive technique used to control this condition is plesiochronous operation.¹² This technique requires "nearly synchronous," yet independently operating, oscillators on either side of the interface. Both the user and terminal clock sources must be sufficiently stable and accurate so as to avoid the need for their continuous synchronization. Expensive cesium beam oscillators with an accuracy, reproducibility, and long-term stability on the order of $\pm 1 \times 10^{-11}$ are typically required. The

discrepancy in bit timing is allowed to build up over many hours or many days depending upon the relative accuracy and stability of the two oscillators. At a specific, prearranged frame or time during that day, the frame timing is realigned or "slipped." However, a certain minimum period between frame timing slips must be maintained and tolerated by the users. The frame timing slip period, S_f (in days), is a function of the bit clock rate, R_b (in bits per second), its stability, WR_b/R_b , and the frame duration, N_f (in bits). Using a conversion of 86 400 s/day:

$$S_f = (1/R_b)(R_b/WR_b)(N_f)(1/86\ 400)$$

For example, a 2.048 Mb/s multiplexed system with a $\pm 10^{-11}$ stable clock and 256 bit frames will experience a frame timing slip about once every 72 days.¹³ During the time set aside for frame timing slips, no user data may be sent. In effect, the network runs asynchronously between timing corrections.

Disadvantages of Plesiochronous Operation

The plesiochronous synchronization technique is very reliable, is easy to expand throughout a growing network, and allows independent, internal synchronization techniques to be employed within subnetworks of international networks. However, plesiochronous operation requires accurate ($\pm 10^{-11}$) and therefore expensive clock sources at each node. For a lower data rate user in a cost efficient satellite network, lower stability clock sources within the user interface equipment are desirable. For example, a terrestrial user connected to the satellite network via a TDMA ground terminal might request a DS1 level service connection with a bit rate of 1.544 Mb/s, a clock stability of $\pm 50 \times 10^{-6}$, and a 193 bit frame.¹⁴ One frame of misalignment could occur about every 30 ms. In a practical system, hundreds or even thousands of frames of misalignment would have to be absorbed before correction could occur.

In plesiochronous operation, the longer the period between timing alignment, the larger the required compression and expansion buffers. The buffers must be sized to accommodate the asynchronism in bit clock timing over the long periods between time alignment. The buffer depth is related to: (1) the minimum acceptable interval between timing slips (which is also a function of path delay variation due to satellite motion and atmospheric and ionospheric conditions); and (2) accumulated timing errors between the clocks on either side of the interface. For this reason, compression and expansion buffers designed for use in the INTELSAT system combine the functions of Doppler effects compensation and plesiochronous timing alignment, and are referred to as alignment and Doppler buffers.¹⁵

Plesiochronous operation requires the most accurate clocks of the various disciplined and nondisciplined synchronization techniques,¹⁶ and controlled timing slips must be allowed to occur periodically. The variable rate compression and expansion buffer technique described in this paper offers the significant advantage of supporting

multiple-user data rates with clocks that are asynchronous with respect to the ground terminal clock, without the disadvantages of expensive clock sources, limited data rate support, frame timing slips, and large buffer size.

Variable Rate Synchronization Technique

Given the brief background on the sources and effects of clock variation on TDMA ground terminals presented above, the implementation approach for the variable-rate technique can now be presented. In this section of the paper, six specific operational objectives are identified, and the details of how the variable-rate compression and expansion buffers meet these objectives are described.

Master-slave disciplined synchronization techniques are used in the SITE ground network and switching transponder simulation. Each ground terminal's transmit and receive counters are indirectly slaved or synchronized to the master clock timing (on board the satellite) through periodic in-band reception of reference bursts from a master control terminal (MCT). The MCT's reference clock is slaved to the onboard master clock. The matrix switch state changes are also synchronous with the onboard master clock.

The transmit side of the terminal accepts the bit clock timing from each source user without any adjustment. There, burst compression buffers (one for each user) absorb the asynchronism between users' clocks and the modulator burst clock. The receive side of the terminal accepts bit clock timing from the demodulator, also without any adjustment. The shallow FIFO buffer following the demodulator absorbs the instantaneous asynchronism between the clocks derived from received bursts and the ground terminal's master clock. The burst expansion buffers (also one for each user) absorb the frame-to-frame fluctuation in valid data fill level so that stable bit clocks can be regenerated and delivered to the destination users.

Note that since received bursts originate from various source terminals in the network, each will exhibit some measure of frequency inaccuracy (associated with the modulator burst clock) and Doppler shifting (unique to the source terminal's uplink range variation). Accordingly, the clocks derived from each successive burst are completely independent in frequency, amplitude, and arrival time. The burst demodulator must be capable of rapid clock recovery and valid data identification.

In the TDMA terminal, the compression and expansion buffers, along with their controllers, are implemented as part of the user interface equipment as shown in the block diagram of Fig. 10. The appropriate compression and expansion buffers are multiplexed onto the transmit and receive data busses, respectively, according to the burst-time plan. The ground terminal's master clock (operating at the modulator burst rate) is used to create both the compression buffer read clock and the expansion buffer write clock.

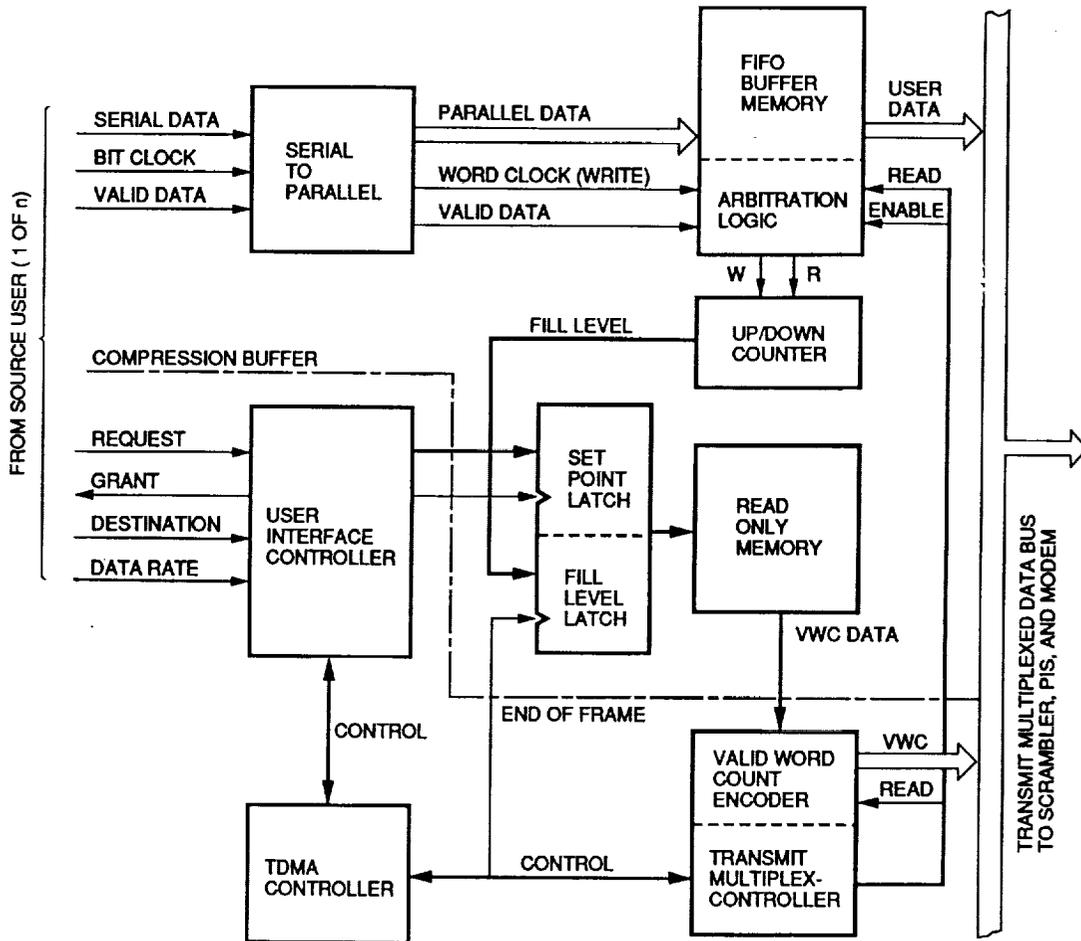


Fig. 10 Block diagram showing one compression buffer (one for each user) and source user interface.

Objectives

The primary objectives in the design of the SITE TDMA terminal compression and expansion buffers were:

- (1) Variable-rate user interface - accommodate user data rates from 256 kb/s to nearly the modulator burst rate of 221.184 Mb/s with asynchronous clocks and minimal stability requirements;
- (2) Clock regeneration - regenerate and deliver to the destination user a bit clock synchronized to the delivered bit stream with equal or better stability than that of the source user clock, while absorbing the effects of modulator oscillator instability and range variation;
- (3) Bit-count integrity - deliver to the destination user exactly the same valid data bit stream that was received from the source user with no lost or duplicated bits (forward error correction is not addressed here) thereby eliminating timing slips;
- (4) Minimal overhead - minimize overhead bits that contribute TDMA frame inefficiency;
- (5) Fixed buffer delay - provide an equal propagation

delay (quantized to an integer number of frame periods) through the TDMA terminal regardless of the user's data rate; and

- (6) Minimum memory requirements - eliminate on-line, off-line (ping-ponged) burst buffer memories in favor of minimal depth FIFO memories.

The mechanisms for satisfying each of these objectives in the design and implementation of compression and expansion buffers are described in the sections that follow.

Variable-User Data Rates

For the compression FIFO buffer, a number of fill-level thresholds (in words) are established over a binary logarithmic scale (powers of two) to cover the ranges of user information data rates. As stated earlier, the compression buffer threshold value must be reached before transmission of valid data bursts can begin. The thresholds are a function of the modulator burst rate, R_m (in bits per second), the TDMA terminal's internal word width, W (in bits per word), and the frame duration, T_f (in seconds per frame). For example, the data rate ranges and thresholds shown in Table 1 are compatible with the SITE TDMA

terminal's 221.184 Mb/s modulator and 64-bit wide serial-to-parallel (S/P) and parallel-to-serial (P/S) converters, operating with a 250 ms TDMA frame period.

TABLE 1. - SUPPORTED USER DATA RATES AND FIFO BUFFER VALUES

Data rate range (Mb/s)	NWC values (words per frame)	Threshold words	Setpoint (hex)
0.256 to 0.512	1 to 2	2	0
.512 to 1.024	2 to 4	4	1
1.024 to 2.048	4 to 8	8	2
2.048 to 4.096	8 to 16	16	3
4.096 to 8.192	16 to 32	32	4
8.192 to 16.384	32 to 64	64	5
16.384 to 32.768	64 to 128	128	6
32.768 to 65.536	128 to 256	256	7
65.536 to 131.072	256 to 512	512	8
131.072 to 221.184 ^a	512 to 1024	1024	9

^aLimited to modulator burst rate.

The user data rates are also grouped into binary logarithmic ranges. For this example, the range limits are powers of two times a base of 1 kb/s, starting with the lowest supported data rate of 256 kb/s. The mapping of user data rates to the binary FIFO threshold levels shown in Table 1 guarantees that any data rate within each range will fill the FIFO to a point greater than the threshold value within three-frame periods regardless of when during the transmit frame the user data stream begins. This threshold feature is necessary to ensure nearly identical buffer delay (nominally two frames' worth) for the full range of supported user data rates. The setpoint is a hexadecimal value used by the TDMA controller to prepare the compression FIFO buffer for operation and to determine the amount of capacity to be requested for connection.

Nominal Word Count

Every supported user data rate, R_u (in bits per second), can be expressed as an equivalent word rate, R_w (in words per frame), by multiplying by the frame duration, T_f , and dividing by the word width, W :

$$R_w = R_u T_f / W$$

The nominal word count (NWC) corresponding to each information rate is defined as the largest integer less than R_w . The NWC represents the approximate number of words received from the source user during each frame. The compression and expansion buffer threshold value is equal to the upper limit of NWC values corresponding to the appropriate data rate range as shown in Table 1.

The TDMA controller of the source terminal sends an orderwire via the satellite to the master control terminal (MCT) requesting a new connection with sufficient capacity to contain a burst a few words larger than the NWC. The requested burst size must accommodate the fractional value of the equivalent word rate and its upper tolerance (due to user clock instability), and the TDMA overhead of preamble and guard times. In practice, capacity is requested and allocated in uniformly-sized subframes to ease burst-time plan generation in a demand-assigned com-

munications network. If sufficient capacity is available, the MCT grants the request and instructs the appropriate destination ground terminal to prepare for a connection with the same capacity between the specific source and destination users. At the destination terminal, the appropriate threshold setpoint is initialized in the expansion buffer based on the NWC received in the orderwire.

Valid Word Count

Once the NWC is known by the destination terminal, only the change from the NWC value need be sent along with each data burst. In the variable-rate buffer technique, this change is called the valid word count (VWC). The VWC can assume four possible values: (1) no words in the burst are valid (transmission has not begun or has ended); (2) a number of words equal to the NWC are valid; (3) a total of one word less than the VWC are valid; and (4) a total of one word more than the VWC are valid. The VWC value is heavily forward-error-correction encoded to ensure correct reception at the destination terminal. In the SITE terminals, the four possible VWC values are encoded into four 12-bit codewords by a simple hardware lookup table called the VWC encoder (see Fig. 10) and inserted into a header that precedes the data portion of each burst (see Fig. 6). For improved TDMA efficiency, either a higher code rate could be used, or more check bits could be assigned to the less-likely-occurring VWC's. If a VWC codeword is not correctable, the value indicating that either the NWC is valid or none are valid is assumed depending upon whether or not valid burst communication has already begun.

Once the compression buffer threshold value has been reached (as observed at the end of each transmit frame), transmission of valid data bursts can begin during the next frame. For an example with the conditions listed in Table 2, the valid data fill level as a function of time is depicted in the graph shown in Fig. 11. Notice that the user's data stream does not need to begin at any specific time during the TDMA frame and that transmission will not begin until the threshold has been reached.

TABLE 2

Parameter	Value
User data rate, Mb/s	1.544
Equivalent word rate, words per frame	6.031
Nominal word count, words	5
Threshold value, words	3
Burst rate (read), words per frame	364
Frame duration, μ s	250

Frame	Starting level	Words written	Words read	Ending level
N	0.000	4.500	0	4.500
N + 1	4.500	6.031	0	10.531
N + 2	10.531	↓	7	17.563
N + 3	17.563		7	24.594
N + 4	24.594		6	30.625
N + 5	30.625		6	36.656

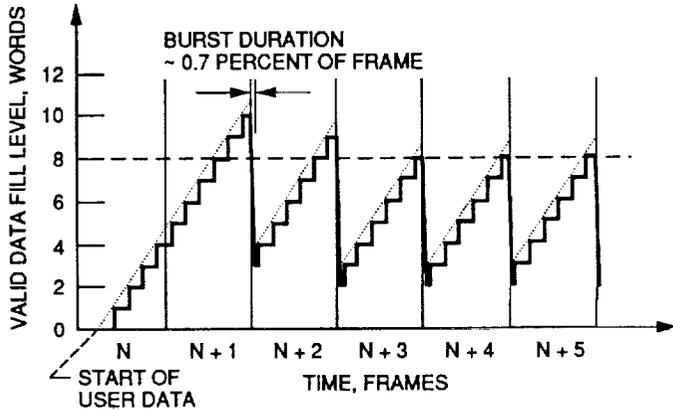


Fig. 11 Compression buffer fill level vs. time for example conditions shown in Table 2.

Most often, successive bursts for the same user will contain either the nominal number of valid words (NWC) or one additional word. The decimal portion of the equivalent word rate, R_w , represents the percentage of time that the transmission of one additional word is necessary to maintain the equivalent throughput of the serial data stream. For example, a user data rate of 1.544 Mb/s has an equivalent 64-bit word rate of 6.03125

words per frame. This means that a burst made up of seven words must be transmitted during 3.125 percent of the frames, while only six words need be transmitted during 96.875 percent of the frames.

Clock Regeneration

At the destination terminal, a $2^{12} = 4096$ word programmable read-only memory (PROM) is used to decode the 12-bit VWC codeword (see Fig. 12). The number of valid words indicated by the combination of the NWC and VWC values is written into the expansion FIFO buffer. A microprocessor-controlled feedback circuit attempts to recreate the exact source user bit clock frequency by observing the fill level of the expansion buffer at the end of each frame and adjusting a VCO frequency accordingly.

Clocks created from the VCO output are used to read data words out of the expansion buffer and align the continuous serial bit stream delivered to the destination user. For an example with the conditions listed in Table 3, the expansion buffer fill level versus time is depicted in Fig. 13.

After the burst-time plan is updated (in preparation for the new user connection to the network), but before either

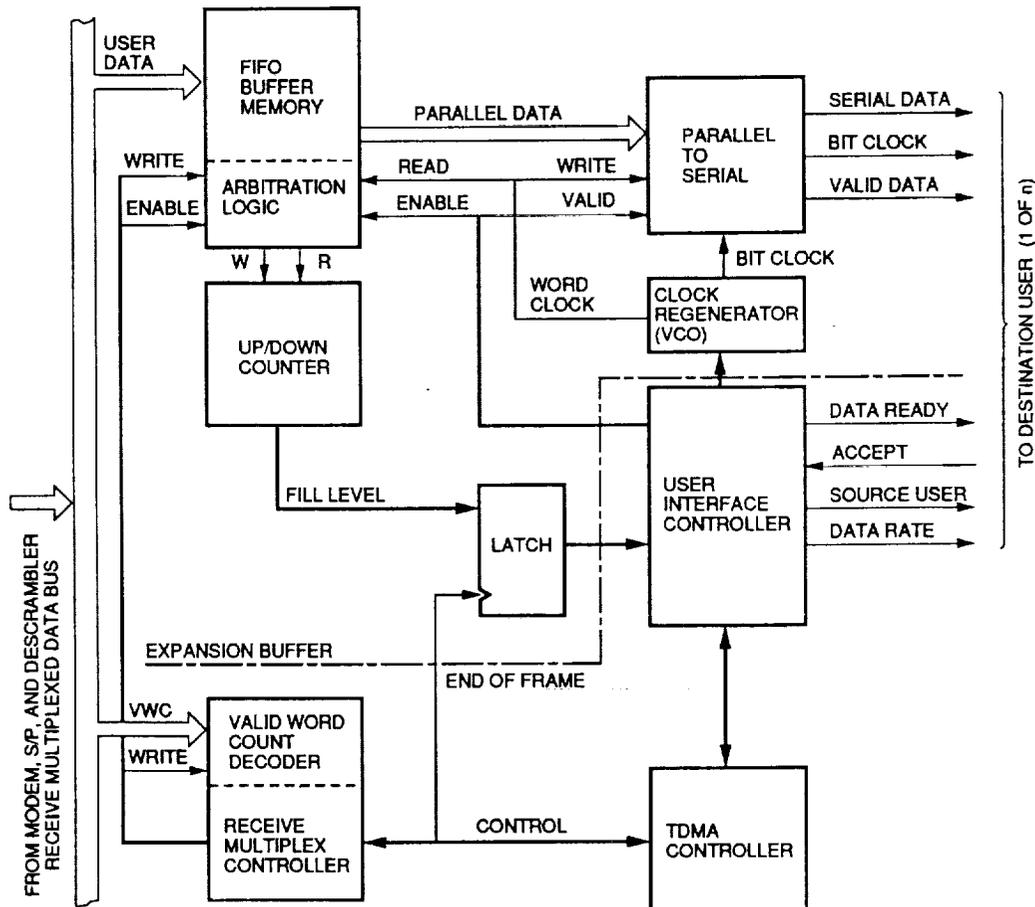


Fig. 12 Expansion buffer/destination user interface block diagram.

TABLE 3

Parameter		Value
User data rate, Mb/s		44.736
Equivalent word rate, words per frame		174.75
Nominal word count, words		174
Threshold value, words		256
Burst rate (read), words per frame		864
Frame duration, μ s		250

Frame	Starting level	Words written	Words read	Ending level
N	0.000	175	0.00	175.00
N + 1	175.00	175	174.75	220.00
N + 2	220.00	175		220.25
N + 3	220.25	174		219.50
N + 4	219.50	175		219.75
N + 5	219.75	175		220.00

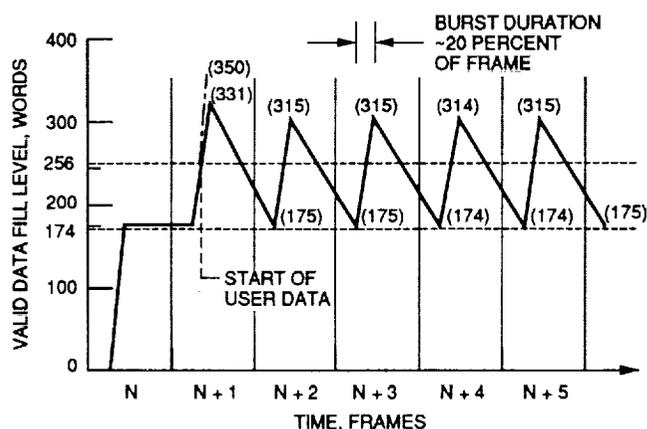


Fig. 13 Expansion buffer fill level vs. time for example conditions shown in Table 3.

the source user's valid data stream begins or the compression buffer reaches the appropriate threshold value, the source terminal sends the VWC codeword indicating that no words are valid. During this time, the clock regeneration loop in the destination terminal creates the frequency that corresponds exactly to the NWC value. Valid source data arriving in the demodulated bursts are accompanied by a VWC codeword other than "none valid." By the end of the second frame after valid data burst reception begins, the expansion buffer threshold level will be reached. At that time, data words begin to be read out of the expansion buffer, are converted to a serial data stream, and then delivered to the destination user with a control signal indicating the start of valid data. At the same time, the VCO loop is enabled to adjust the frequency of the buffer read word clock and the synchronous user bit clock.

For the SITE terminals, a clock regeneration loop was designed to use a single 200.000 MHz VCO to create a variety of binary submultiple data rates: 100, 50, 25, 12.5, and 6.25 Mb/s for demonstration purposes. The clock

regeneration software is executed on the user interface controller microcomputer that executes the connection protocol between the users and the ground terminal. For a description of the user interface controller see Ref. 17. The clock regeneration subroutine reads the expansion FIFO buffer levels at the end of each frame, determines an appropriate subtle frequency correction, and applies the proper voltage to the VCO. In future versions, a numerically controlled oscillator (NCO) or a direct digital synthesizer (DDS) may be used for clock regeneration. Details of the user clock regeneration technique will be the subject of a future paper.

Bit-Count Integrity

The source and destination terminals are required to maintain bit-count integrity; that is, every valid data bit is transferred from source to destination user in exactly the order received. Once the source user's request for connection with a specific data throughput has been granted, the source terminal places no restrictions on when the valid data stream can start. However, the user is required to indicate the start of valid data with a separate control line. The S/P converter in the ground terminal user interface uses this control signal to allow only valid data words to be written into the compression buffer. Since there are no restrictions on when the valid data may arrive relative to transmit frame timing, it may take more than the minimum number of frames possible for the threshold value to be reached at that data rate. In any case, the source terminal will wait until a full burst of valid data is available and then mark it as such with the appropriate VWC codeword.

A similar situation exists in the expansion buffer where no demodulated bursts of data are written until the VWC codeword indicates the data are valid. By observing the compression and expansion buffer fill levels at the same relative instant from frame to frame, data processing can begin during the earliest possible frame. Valid data words read out of the expansion FIFO memory are converted to a serial stream by a P/S converter. Here, the user interface controller must indicate to the P/S converter exactly when valid data words are being read. The P/S converter changes the state of a valid data control signal to indicate to the destination user the start of valid serial data.

Because this variable-rate buffer technique absorbs the asynchronism between the users' and the terminal's clocks, and smooths the regenerated clock to approach the equivalent data throughput, no timing slips are created. The same valid data sequence sent by the user and received by the source terminal is delivered to the destination user with no additional or deleted bits and with nearly the identical frequency of the source user's bit clock.

TDMA Frame Efficiency

TDMA frame efficiency, defined as the ratio of the number of information-carrying bits per frame over the total number of bits per frame, is a function of network

and terminal "overhead" (in-band command/status communications, burst demodulator preamble, and guard times (see Fig. 6)), and the frame duration. Longer bursts with fewer overhead bits in longer frames yield higher TDMA frame efficiency. To support very low rate (tens to hundreds of kilobits per second) voice, data, and video users in an efficient TDMA network, a frame duration of 30 ms or longer is desirable. For unidirectional video transmission and low-rate data transfer, interframe multiplexing of user data can also be used to improve frame efficiency. In interframe multiplexing, user data accumulate over several frames until one reasonably efficient burst can be assembled and transmitted. In this way, the same time slot in a frame can be time-shared by several low-data-rate users attached to a TDMA terminal.

The variable-rate compression and expansion buffer technique has an effect on TDMA frame efficiency. The number of bits allocated for the VWC codeword contributes to the overhead and thereby decreases TDMA efficiency. The technique also requires that additional words beyond the NWC be allocated in the burst-time plan. An allocation of NWC plus two words could even be required to accommodate equivalent word rates close to the upper limits of a data range with low stability clock sources. The impact on frame efficiency is traded against the ability to support a continuum of user data rates, and it becomes less severe as word size (which quantizes the user data rate) decreases from 64 bits to a more manageable 8 or 16 bits. The overhead becomes part of the excess allocation within a subframe when uniform subframe multiples are used to partition the frame.

In general, the smaller the word size used and the fewer the number of bits in the VWC codeword, the smaller the impact on frame efficiency. Since the VWC only has to indicate one of four conditions, only 2 bits are absolutely required. Additionally, given the current speed of digital circuitry, an internal word width of 16 or even 8 bits is practical even for burst rates of several hundred megabits per second. Consequently, the effect of this technique on TDMA frame efficiency can be minimal.

Buffer Latency

Recall that compression and expansion buffers that do not support programmable threshold setpoints require that all user data, regardless of the data rate, must be delayed in buffers designed for the maximum user data rates until the half-full condition was reached. This was necessary to accommodate variations in burst timing as the satellite range delay varied. Without waiting for the half-full condition to occur, the buffers would at some point underflow or overflow and thereby destroy user data. The impact of delaying user data in the compression and expansion buffers becomes severe for low-data-rate users since it may take hundreds of TDMA frames before transmission can begin.

By using the variable-rate burst compression and expansion buffer technique, the fill level is set according to the

user's data, thus minimizing data latency within the ground terminal. Each data rate experiences the same throughput delay as all others. The delay for each buffer is either two or three frames, depending upon whether the data rate is in the high or low half of the data rate range (see Table 1), and depending upon when the source user data sequence begins relative to the transmit frame timing. By minimizing the expansion buffer depth necessary to accommodate variable data rates that are asynchronous with respect to the ground terminal's clock, the propagation delay of user data in the ground terminal is also minimized. Furthermore, without a clock regeneration technique, large expansion buffers would be necessary and asynchronous user data could be delayed in the expansion buffer for several seconds. Such latency would clearly be unacceptable for most interactive communications applications.

Memory Requirements

As noted in the introductory section, the ping-pong memory approach consumes twice as much memory as the FIFO memory approach. For the SITE terminals, a nearly identical pair of 2048-word-deep by 64-bit-wide FIFO buffer memories was developed for use as both the compression and expansion buffers for each user (see Fig. 14). The FIFO buffer boards were initially designed and fabricated in-house as an array of conventional, single-port random access memories (RAM) controlled by arbitration logic constructed from combinational and sequential logic circuits. Since these buffers were designed, commercial FIFO memory chips with serial and parallel interfaces and 2048-word depth have become available. Future designs will be based on 16-bit-wide interfaces and may exploit the features of commercial, self-contained FIFO chips or multiported RAM and FIFO RAM controller chips.

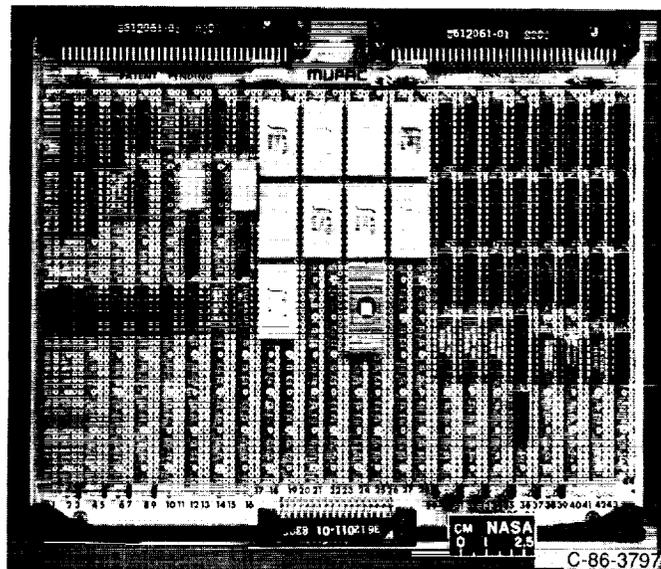


Fig. 14 Prototype compression/expansion FIFO buffer board.

The total amount of memory required, M_t (in bits), is simply two times the highest user data rate supported

(including its upper tolerance measured over one-frame period), R_b (in bits per second), times the frame duration, T_f (in seconds) $M_t = 2R_b T_f$. The factor of two is required only if the valid user data stream is allowed to start asynchronously with respect to the transmit frame timing. If a user with a data rate near the upper limit of any data rate range (see Table 1) just misses reaching the compression buffer threshold near the end of one frame, then nearly twice as many words as the threshold value will be ready for transmission by the same time in the next frame. If users' data transmissions were restricted to start coincident with some source terminal timing signal, then only half as much FIFO memory is required. Following the earlier discussion of range delay, absolute and variable range delay parameters do not enter into the total memory equation.

The chip implementation of the total memory required is a function of the data word width internal to the terminal and the modulator burst rate. These two parameters determine the memory cycle time required and the word width and depth of each chip. Using word widths greater than 1 bit reduces the required memory cycle time but necessitates the use of serial-to-parallel converters when the user interface is serial.

The absolute memory requirements for this technique are small. Note that the FIFO memory must support external selection of a variety of thresholds and provide sufficient output information to indicate instantaneous fill level. These features are used in both the compression and expansion buffers. Many commercially available FIFO memories have no externally settable thresholds, and can only indicate full, nearly full, half, nearly empty, and empty conditions. Other features available in some commercial FIFO memories include built-in serial and parallel interfaces, the ability to be cascaded in depth with no additional logic, multiple threshold setpoints and indicator flags, and programmable operation. FIFO memories with enhanced features and performance are regularly introduced because of their application in the rapidly growing digital signal processing and multiprocessor design fields. A variable-rate burst compression and expansion subsystem for future TDMA ground terminals could quite possibly consist of two fully featured, single-chip FIFO memories per user and a microcontroller-based direct digital synthesizer.

Concluding Remarks

In this paper, a new technique was described for accommodating a variety of asynchronous user data rates in an SS/TDMA network. The sources of clock variation and the mechanisms to accommodate them were addressed. Through the use of nominal and valid word counts, FIFO memories, frame-duration adjustment, and microprocessor-controlled clock regeneration, the variable-rate compression and expansion buffer technique provides bit-count integrity and minimal data latency to low and medium data rate users not traditionally supported by SS/TDMA networks. The variable-rate compression and expansion

buffer technique can be readily extended to much lower and higher information bit rates, none of which need be synchronous with any other clocks in the system. The technique offers the flexibility for variable data rate users to operate in an SS-TDMA network with minimal terrestrial interface equipment cost. Finally, the technique enables users with a wide variety of asynchronous interface protocols to conduct network experiments via the ACTS HBR segment.

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16. Abstract A burst compression and expansion technique is described for asynchronously interconnecting variable-data-rate users with cost-efficient ground terminals in a satellite-switched, time-division-multiple-access (SS/TDMA) network. Compression and expansion buffers in each ground terminal convert between lower rate, asynchronous, continuous-user data streams and higher-rate TDMA bursts synchronized with the satellite-switched timing. The technique described uses a first-in, first-out (FIFO) memory approach which enables the use of inexpensive clock sources by both the users and the ground terminals and obviates the need for elaborate user clock synchronization processes. A continuous range of data rates from kilobits per second to that approaching the modulator burst rate (hundreds of megabits per second) can be accommodated. The technique was developed for use in the NASA Lewis Research Center System Integration, Test, and Evaluation (SITE) facility. Some key features of the technique have also been implemented in the ground terminals developed at NASA Lewis for use in on-orbit evaluation of the Advanced Communications Technology Satellite (ACTS) high burst rate (HBR) system.				
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